tions and oxidizing exposure time. Accordingly, the above exemplary width can be varied depending upon the desired application.

Turning now to FIG. **7**, a processing step is shown whereby a fill dielectric **56** is deposited upon and between the converted silicon risers **54** and partially consumed silicon mesas **43**. Fill dielectric **56** is preferably an LPCVD-deposited TEOS or an atmospheric-pressure ozone-TEOS material blanket deposited across the entire wafer topography. It is understood that fill dielectric **56** may comprise several applications of dielectric material (preferably oxide) in order to fill trenches between consumed silicon risers **54** and mesas **43**.

FIG. **8** illustrates a planarization step which occurs subsequent to the step shown in FIG. **7**. More specifically, fill dielectric **56** is partially removed at its upper regions from an elevational level **58** to an elevational level **60**. Elevational level **60** resides below recesses **59**, and is substantially level across converted silicon risers **54** and mesas **43**. Planarization is performed using chemical-mechanical polishing (CMP). CMP is effective in producing a substantially planar surface since recesses **59** are minimal as a result of the close spacing between silicon risers **54**. Accordingly, silicon risers **54** in wide field areas ensure that the deposited topography of fill dielectric has many small recesses, rather than one large recess. A large recess is problematic in CMP since a large recess can not in all instances be removed, or planarized. Recess **59** preferably comprises a lateral dimension substantially equal to the width of an underlying trench. The vertical dimension of recess **59** is also proportional to the width of the trench, wherein trench width is, according to a preferred embodiment, of uniform dimension across the semiconductor substrate. By ensuring that spacings between silicon riser **54** is of approximately the same width, the present process can control the recess dimension and thereby achieve substantial planarity through CMP.

FIG. **9** illustrates a processing step subsequent to that of FIG. **8**. Shown as a unitary dielectric material, comprising fill dielectric and grown dielectric, a field dielectric **62** is shown. Field dielectric is formed as a result of complete consumption of silicon risers **54**, and the deposition of fill dielectric **56** between the consumed risers. Field dielectric **62** is dimensioned having a width extending between silicon mesas **43** (between active regions). Field dielectric **62** also has a thickness extending from the bottom of silicon trenches formed in the step shown in FIG. **4** to the elevation **60** shown in FIG. **8**. Deposited and subsequently patterned upon field dielectric **62** is a conductor **64**. Conductor **64** is electrically conductive, and can be made of either a refractory metal or polysilicon. Conductor **64** may also be formed above partially consumed active regions **43**, and thereby forms a gate conductor **66**. Gate conductor **66** and field conductor **64** can be formed from the same conductive layer, possibly as the first level of interconnect within numerous levels of interconnect. Conductor **64** is used to connect isolated devices found within active regions **43**.

FIG. **10** illustrates, according to an alternative embodiment, silicon risers **68**. Silicon risers **68** are not consumed by an oxidizing ambient, as in the embodiment shown in FIG. **6**. Instead, silicon risers **68**, as well as silicon mesas **42** extend upward into the fill dielectric **62**. Fill dielectric **62** is subsequently planarized by removing recesses **59**, similar to the step shown in FIG. **8**. A distinction, however, between the steps of FIG. **8** and FIG. **10** is the amount by which fill dielectric **62** upper surface is removed, or planarized. In FIG. **10**, CMP occurs to an elevational depth below recesses **59** but well above the upper surfaces of silicon mesas **42** and silicon risers **68**. The planarization level **70** is chosen such that sufficient dielectric thickness exist between the silicon upper surfaces and any overlying conductors, such as a conductor placed upon the planarized surface **70**.

It will be appreciated to those skilled in the art having the benefit of this disclosure that this invention is capable of applications with numerous types of MOS-processed circuits. Furthermore, it is to be understood that the form of the invention shown and described is to be taken as presently preferred embodiments. Various modifications and changes may be made to each and every processing step as would be obvious to a person skilled in the art having the benefit of this disclosure. It is intended that the following claims be interpreted to embrace all such modifications and changes and, accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. A method, as part of a MOS trench isolation process, for planarizing a field dielectric between a widely spaced pair of active regions, comprising:

providing a spaced pair of active regions within a silicon substrate;

forming a protective layer upon said silicon substrate;

depositing a photoresist upon said protective layer;

polymerizing select areas of said photoresist layer;

removing intermittent regions of said photoresist layer, said protective layer, and said silicon substrate between said pair of active regions to form a spaced set of silicon risers extending from said silicon substrate, wherein said spaced set of silicon risers is defined by said select areas of said photoresist layer, and wherein said silicon risers comprise portions of said silicon substrate that have not previously been subjected to an implantation process associated with active devices;

removing remaining portions of said photoresist layer, wherein said remaining protective layer prevents grown oxidation on top surfaces of said active regions and said spaced set of silicon risers;

depositing a field dielectric upon and between said silicon risers to produce a field dielectric topography having recesses between respective silicon risers;

removing said field dielectric topography to an elevational level below said recesses and above said silicon risers; and

forming at least one MOS device in each of said pair of active regions.

2. The method as recited in claim **1**, wherein the step of removing said intermittent regions comprises etching 0.2 to 1.0 microns of said silicon substrate within said intermittent regions.

3. The method as recited in claim **1**, wherein said depositing step comprises chemical vapor depositing from a tetraethoxysilane source.

4. The method as recited in claim **1**, wherein said depositing step comprises chemical vapor depositing from a tetraethoxysilane and ozone source.

5. The method as recited in claim **1**, wherein said depositing step comprises depositing said field dielectric from within a low pressure chemical vapor deposition chamber.

6. The method as recited in claim **1**, wherein said removing said field dielectric topography comprises chemical mechanical polishing.

7. The method as recited in claim **1**, wherein said active regions comprise silicon mesas having an upper surface substantially equal to an upper surface of said silicon risers.